

AMENDMENTS TO THE CLAIMS

1. (original): A cross-connection switch comprising:

first memory means for storing data indicating switching information of a time slot at an address to which time slot information is assigned;

second memory means for storing data of each time slot of an input frame in time slot units, inputting data stored in said first memory means, and outputting the data stored at the address specified by the data as time slot data of an output frame; and

counter means for counting a number of input time slots of an input frame, and outputting the count value as a read address and a write address respectively to said first memory means and said second memory means.

2. (original): The switch according to claim 1, wherein

when a multiplexed line signal having an input frame of n bits per channel is processed, a time slot number of each bit of an n -bit channel is assigned to addresses of said first memory means, and data indicating switching information about a time slot of each piece of bit data is entered at each address of said second memory means.

3. (original): The switch according to claim 1, wherein

when a plurality of lines are accommodated by said cross-connection switch, any line of the plurality of lines is selected for a switching process by entering switching information about time order of data of a time slot and switching information data between lines at each address of said first memory means.

4. (original): The switch according to claim 1, wherein

information of a current input time slot is written to said second memory means, data to be used in processing one time slot before the current input time slot is read from said first memory means, a read address is output from said first memory means to said second memory means, and time slot data used in processing the one time slot before the current input time slot is read from said second memory means.

5. (original): The switch according to claim 1, further comprising

selector means for switching data of a time slot directly input from an input line with data of a time slot read from said second memory means and outputting a switching result, wherein

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said selector means is controlled to output time slot information not to be switched as time slot data of an output frame without performing a process on the information by inputting information read from said first memory means as a selector signal to said selector means, and to output time slot data read from said second memory means as time slot data of an output frame to be switched.

6. (original): The switch according to claim 5, further comprising

flipflop means for holding data of a time slot read from said second memory means, wherein

a timing of a switching process of said selector means is adjusted by inputting to said flipflop means a second clock generated by adjusting a phase of a first clock synchronous with a time slot of an input frame by inputting to said flipflop means time slot data used as data of one time slot earlier than a current point from said second memory means.

7. (original): The switch according to claim 6, further comprising

phase adjustment means for inputting the first clock, and generating the second clock whose phase is faster than the first clock by a predetermined time with an output delay of said flipflop means and a switching delay of said selector means taken into account, wherein

said output delay and said switching delay are absorbed by inputting the second clock generated by said phase adjustment means as a clock signal to said flipflop means.

8. (newly added): A cross-connection switch comprising:

A/ a counter counting a number of input time slots of an input frame, and outputting the count value as a read address and a write address;

a first memory storing switching information data for a time slot, said data stored corresponding to addresses to which time slot information is assigned and outputting said switching information data according to the read address from said counter;

a second memory storing data of each time slot of an input frame in time slot units according to the write address from said counter and outputting said stored data of each time slot as read utilizing the switching information data from said first memory as a read address, thereby outputting time slot data of an output frame.